**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (currently amended): A method of fabricating an integrated circuit, the integrated circuit having a semiconductor body, the method comprising following steps:

(a) forming a plurality of basic units on the semiconductor body, each of the basic units having an identical ~~device characteristic~~ structure; and

(b) forming at least a layout layer to program the basic units for generating a clocked logic circuit and a non-clocked logic circuit without placing restrictions on positions of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body[[.]] ;

wherein the clocked logic circuit comprises at least two of the basic units of which at least one of the at least two basic units is programmed to be isolated from a clock feed.

Claim 2 (original): The method of claim 1 wherein step (a) forms at least a transistor within each of the basic units.

Claim 3 (original): The method of claim 2 wherein the transistor is an MOS transistor.

Claims 4 (cancelled)

Claim 5 (original): The method of claim 1 wherein step (b) utilizes the layout layer to program a plurality of basic units for generating the clocked logic circuit.

Claim 6 (original): The method of claim 1 wherein step (b) utilizes the layout layer to

program a basic unit for generating the non-clocked logic circuit.

Claim 7 (original): The method of claim 1 wherein step (b) utilizes the layout layer to program a plurality of basic units for generating the non-clocked logic circuit.

Claim 8 (original): The method of claim 1 wherein step (a) forms at least a PMOS transistor and at least an NMOS transistor within each of the basic units.

Claims 9-14 (cancelled)

Claim 15 (currently amended): An integrated circuit comprising:

a semiconductor body for positioning a plurality of basic ~~unit~~ units, each of the basic units having an identical ~~device characteristic~~ structure;

a clocked logic circuit formed on the semiconductor body, the clocked logic circuit being formed by at least [[a]] one of the basic ~~unit~~ units; and

a non-clocked logic circuit formed on the semiconductor body, the non-clocked logic circuit being formed by at least one of the basic ~~unit~~ units;

wherein the clocked logic circuit comprises at least two of the basic units of which at least one of the at least two basic units is programmed to be isolated from a clock feed.

~~wherein the semiconductor body does not limit locations of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body.~~

Claim 16 (original): The integrated circuit of claim 15 wherein each of the basic units comprises at least a transistor.

Claim 17 (original): The integrated circuit of claim 16 wherein the transistor is a MOS

transistor.

Claim 18 (original): The integrated circuit of claim 15 wherein each of the basic units comprises at lease a PMOS transistor and at least an NMOS transistor.

Claims 19-22 (cancelled)

Claim 23 (new): A method of fabricating an integrated circuit, the method comprising the following steps:

forming a plurality of basic units on a semiconductor body, each of the basic units having a first row of transistors cascaded in a series and a second row of transistors cascaded in a series;

forming at least a layout layer to program traces among the first row of transistors and the second row of transistors of at least a first basic unit; and

forming a clocked logic circuit by at least two of the basic units of which at least one of the at least two basic units is programmed to be isolated from a clock feed.

Claim 24 (new): The method of claim 23 wherein forming a clocked logic circuit comprises:

programming at least one of the basic units to form a plurality of logic gates isolated from the clock feed; and

programming at least one of the other basic units to receive the clock feed, such that at least one of the transistors in the basic unit is connected to the clock feed.

Claim 25 (new): The method of claim 23 further comprising:

while programming at least one of the basic units isolated from the clock feed, forming at least one logic signal input port by connecting gates of at least one

transistor of the first row and at least one transistor of the second row, and forming at least one logic signal output port by connecting drains of at least one transistor of the first row and at least one transistor of the second row,

and

programming at least one of the other basic units to receive the clock feed by programming at least one transistor in the basic unit such that the at least one transistor have a gate connected to receive the clock gate, and a drain or a source connected to the logic signal input port or the logic output port.

Claim 26 (new): An integrated circuit comprising:

a semiconductor body for positioning a plurality of basic units, each of the basic units having a first row of first transistors cascaded in a series and a second of second transistors cascaded in a series;

a layout layer comprising traces among the first row of transistors and the second row of transistors of at least one of the basic units; and

a clocked logic circuit comprising at least two of the basic units of which at least one of the at least two basic units is programmed to be isolated from a clock feed by the layout layer.

Claim 27 (new): The integrated circuit of claim 26 wherein the layout layer further comprises traces so that a gate of a first transistor of the first row of transistors is coupled to a gate of a first transistor of the second row of transistors, a gate of a second transistor of the first row of transistors is coupled to a gate of a third transistor of the second row of transistors, and a gate of a third transistor of the first row of transistors is coupled to a gate of a second transistor of the second row, a source of the first transistor of the first row of transistors is coupled to a high voltage source, a source of the first transistor of the second row of transistors is coupled to

ground, a source of the second transistor of the first row of transistors is coupled to a source of the second transistor of the second row of transistors, a source of the third transistor of the first row of transistors is coupled to a source of the third transistor of the second row of transistors, a drain of the third transistor of the first row of transistors is coupled to a drain of the third transistor of the second row of transistors, the gate of the third transistor of the first row of transistors is coupled to a system clock, and the gate of the third transistor of the second row of transistors is coupled to an inversion of the system clock.

Claim 28 (new): The integrated circuit of claim 26 wherein the first row of transistors of each basic unit is PMOS transistors, and the second row of transistors of each basic unit is NMOS transistors.